Revision History

Rev. No.	History	Issue Date
1.0	1. New Release. 2. Product Process change from 90nm to 65nm 3. The device build in Power Saving mode as below : 3-1. Deep Power Down (DPD) 3-2. Partial Array Refresh (PAR) 3-3. Temperature Controlled Refresh (TCR),	Mar.27, 2013

■ Product Description

The CS26LV64173 is a high performance, high speed, low power Pseudo SRAM organized as 4,194,304 words by 16 bits and operates from a wide range of 2.7 to 3.6V supply voltage. Advanced DRAM technology and circuit techniques provide both high speed and low power features with a maximum standby current of 180uA and maximum access time of 70ns in 2.7 to 3.6V operation.

The CS26LV64173 available package type is 48-pin BGA.

The device includes several Power Saving modes : Temperature Controlled Refresh (TCR), Partial Array Refresh (PAR) and Deep Power Down (DPD). Both these modes reduce standby current.

The efficient Page Read Mode, data can be read by only changing A0-A3 when A4-A21 is fixed, while /CE1=L, CE2=H, /WE=H, /OE=L, /UB=L, /LB=L.

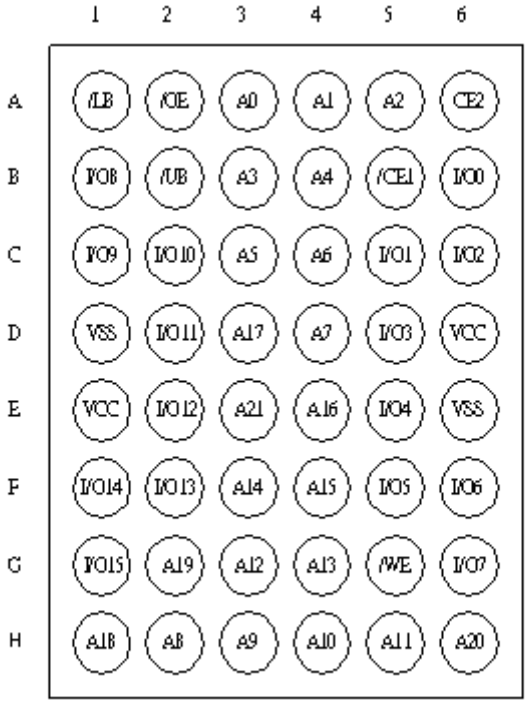
■ Features

- Low operation voltage: 2.7 ~ 3.6V
- Ultra low power consumption:
  - 50mA@14MHz (Max.) Operating Current
  - 180uA (Max.) CMOS Standby Current
- High speed access time: 70ns (Max.)
- Power Saving modes
  - Temperature Controlled Refresh (TCR)
  - Partial Array Refresh (PAR)
  - Deep power down (DPD)

■ Product Family

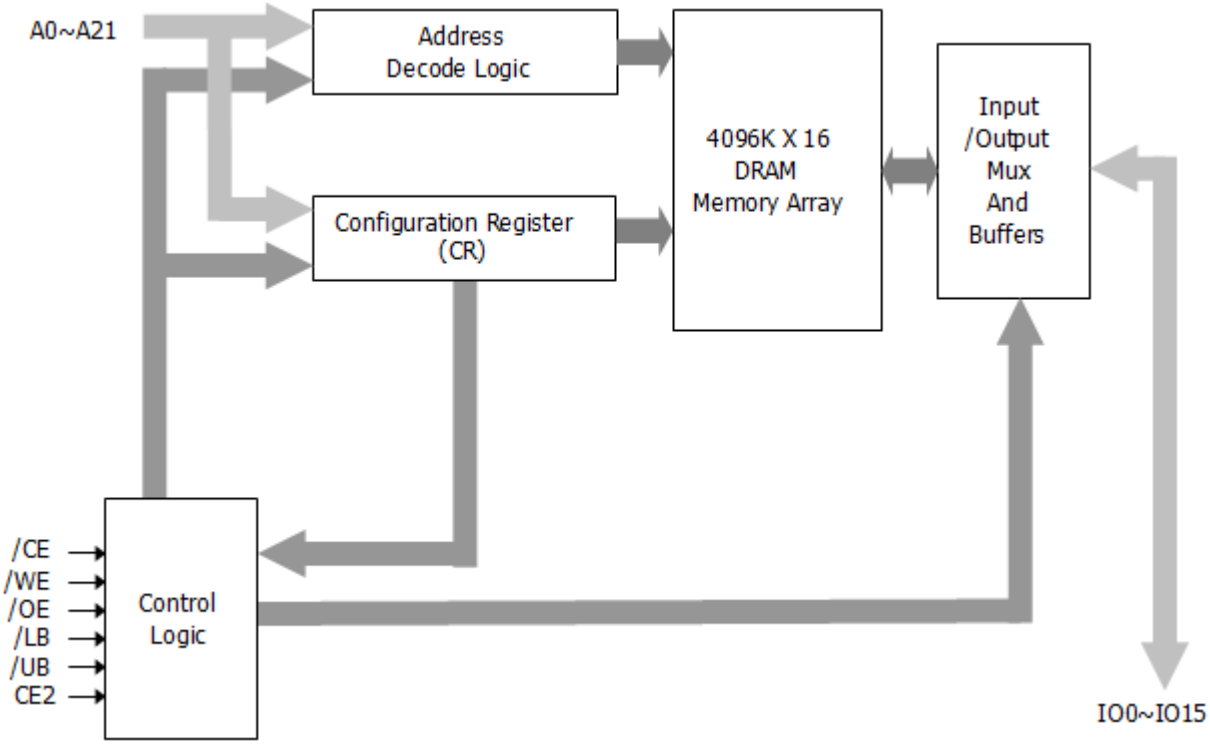
Product Family	Operating Temp	V_{CC} Range	Speed (ns)	Standby (Max.)	Package Type
CS26LV64173	0~70°C	2.7~3.6	70	180 uA	Dice
	-40~85°C				48 BGA-6x8mm

■ Pin Configuration



48 Ball CSP - Top View

■ Functional Block Diagram



■ Pin Description

Name	Type	Function
A0 ~ A21	Input	A0~A3, page address inputs, while A4~A21 address inputs
/CE1 & CE2	Input	Chip enables must be active when data read from or write to the device. if chip enable is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high impedance state when the device is deselected.
/WE	Input	The write enable input is active LOW and controls read and write operations. With the chip selected, when /WE is HIGH and /OE is LOW, output data will be present on the DQ pins; when /WE is LOW, the data present on the DQ pins will be written into the selected memory location.
/OE	Input	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when /OE is inactive.
/LB and /UB	Input	Lower byte and upper byte data input/output control pins.
IO0-IO15	I/O	These 16 bi-directional ports are used to read data from or write data into the RAM.
V_{CC}	Power	Power Supply
V_{SS}	Power	Ground

■ Truth Table

Mode	Vcc	/CE	CE2	/WE	/OE	/UB & /LB	IO[0:15] [4]	Note
Standby	Standby	H	H	X	X	X	High-Z	2,5
Read	Active	L	H	H	L	L	Data-Out	1,4
Write	Active	L	H	L	X	L	Data-In	1,3,4
No operation	Idle	L	H	X	X	X	X	4,5
PAR	Power Saving	H	L	X	X	X	High-Z	6
DPD	Power Saving	H	L	X	X	X	High-Z	6
Load Configuration register	Active	L	L	L	X	X	High-Z	

Notes

1. When /UB and /LB are in select mode (LOW), IO0~IO15 are affected as shown. When only /LB is in select mode, IO0~IO7 are affected as shown. When only UB# is in select mode, IO8~IO15 are affected as shown.
2. When the device is in standby mode, control inputs (/WE, /OE), address inputs, and data inputs/outputs are internally isolated from any external influence.
3. When /WE is active, the /OE input is internally disabled and has no effect on the I/Os.
4. The device will consume active power in this mode whenever addresses are changed.
5. Vin=Vcc or 0V, all device pins be static (unswitched) in order to achieve standby current.
6. DPD is enabled when configuration register bit CR [4] is "0"; otherwise, PAR is enabled.

■ Absolute Maximum Ratings(Note)

Symbol	Parameter	Rating	Unit
V_{CC}	Power supply voltage	-0.2 to 3.6	V
V_{IN}	Input voltage	-0.2 to 3.6	V
V_{OUT}	Output voltage	-0.2 to 3.6	V
T_{BIAS}	Temperature Under Bias	-40 to +85	^{O}C
T_{STG}	Storage Temperature	-55 to +150	^{O}C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

■ DC Electrical Characteristics (Ta = -40 to +85°C , V_{CC} = 2.7 to 3.6V)

Parameter Name	Parameter	Test Conduction	MIN	TYP	MAX	Unit
V_{IL}	Input Low Voltage (1)		-0.2		0.2*Vcc	V
V_{IH}	Input High Voltage (1)		0.8*Vcc		Vcc+0.2	V
I_{IL}	Input Leakage Current	V_{CC}=MAX, V_{IN}=0 to V_{CC}	-1		1	uA
I_{OL}	Output Leakage Current	V_{CC}=MAX, /CE=V_{IH}, CE2=V_{IH}, /OE=V_{IH} or /WE=V_{IL}, V_{IO}=0V to V_{CC}	-1		1	uA
V_{OL}	Output Low Voltage	V_{CC}=MIN, I_{OL} = 0.5mA			0.2*Vcc	V
V_{OH}	Output High Voltage	V_{CC}=MIN, I_{OH} = -0.5mA	0.8*Vcc			V
I_{CC1}	Operating Power Supply Current	Cycle time=1us, I_{IO}=0mA, 100% duty, /CE1≦0.2V, CE2≧V_{CC}-0.2V, V_{IN}≧V_{CC}-0.2V or V_{IN}≦0.2V			5	mA
I_{CC2}		Cycle time=Min, I_{IO}=0mA, 100% duty, /CE1=V_{IL}, CE2=V_{IH}, V_{IN}= V_{IL} or V_{IH}			50	mA
I_{CCP}	Page Access Operating Current	/CE1≦V_{IL}, CE2≧V_{IH} , F=F_{MAX} (2) I_{IO}=0mA , Page add. Cycling			25	mA
I_{CCSB}	Standby Current -CMOS	/CE1 & CE2≧V_{CC}-0.2V, Other pins=0V ~ Vcc			180	uA
I_{CCSBP}	Power Saving Standby Current	CE2≦0.2V, Other inputs=0V ~ Vcc (Max. condition : Vcc=3.6V @ 85℃)			10	uA

Notes:

1. Input signals may overshoot to Vcc + 1.0V for periods less than 2ns during transitions
   Input signals may undershoot to Vss – 1.0V for periods less than 2ns during transitions.
2. $F_{max} = 1/t_{RC}$.

■ Capacitance (1) (Ta = 25°C, f =1.0 MHz)

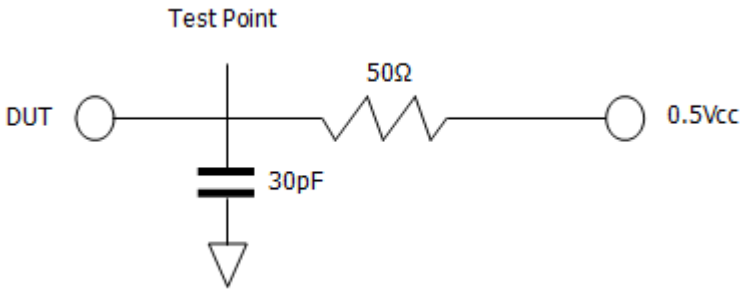
Symbol	Parameter	Conditions	MAX.	Unit
C_{IN}	Input Capacitance	V_{IN}=0V	6.5	pF
C_{DQ}	Input/Output Capacitance	$V_{I/O}$=0V	6.5	pF

1. This parameter is guaranteed and not 100% tested.

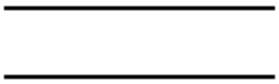
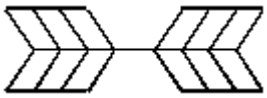
■ AC Test Conditions

Input Pulse Levels	V_{CC}-0.2V/0.2V
Input Rise and Fall Times	5ns
Timing Reference Level	0.5*V_{CC}
Output Load(See right)	CL[1)]=30pF

1. Including scope and Jig capacitance.



■ Key To Switching Waveforms

Waveform	Inputs	Outputs
	Must be standby	Must be standby
	May change for H to L	Will be change from H to L
	May change for L to H	May change for L to H
	Don't care any change permitted	Change state unknown
	Does not apply	Center line is high impedance "OFF" state

■ AC Characteristics

▪ Configuration Registers Operation

The configuration Register (CR) defines how the PSRAM device performs a transparent self refresh. Altering the refresh parameters can dramatically reduce current consumption during standby mode.

Also Page mode is embedded in the CR.

This register can be updated any time the device is operating in a standby state.

The control bits used in the CR are shown in Table 1. At power-up, the CR default value is set to 0070h.

Table 1. Configuration Register

Bit Number	Definition	Remark
21 – 8	Reserved	All Must be set to "0"
7	Page	0 = Page mode disabled (default) 1 = Page mode enabled
6–5	TCR	1 1 = +85°C (default) 0 0 = +70°C 0 1 = +45°C 1 0 = +15°C
4	Sleep	0 = DPD enabled 1 = PAR enabled (default)
3	Reserved	Must be set to "0"
2–0	PAR(1)	000 = Full array (default) 100 = None of array

Notes :

1. Use of other setting will result in full-array refresh coverage.

▪ Access Using CE2

The CR can be loaded using a WRITE operation immediately after CE2 makes transition from HIGH-to-LOW (see Figure 2).

The values placed on addresses A[21:0] are latched into the CR on the rising edge of /CE or /WE, whichever occurs first. /LB and /UB are "Don't Care." Access using CE2 is WRITE only.

Figure 1: Load Configuration Register Operation Using CE2

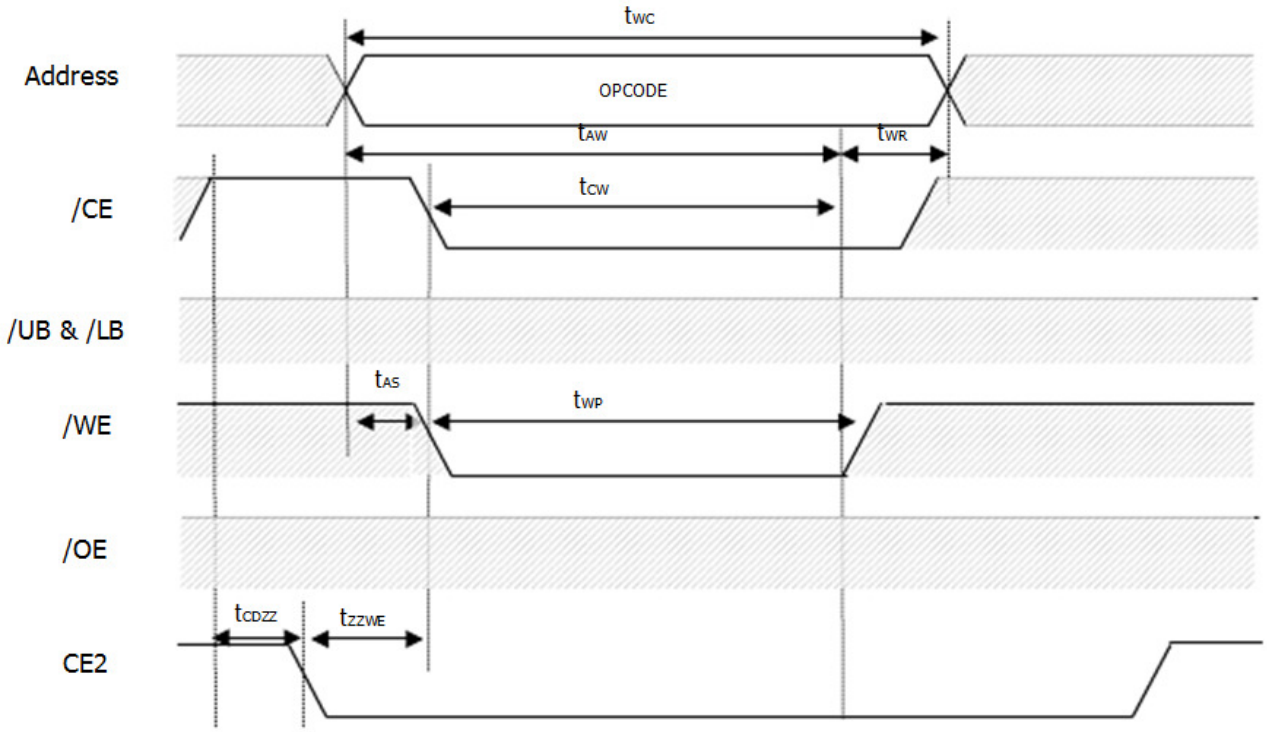


Table 2 . Load Configuration Register Timing Requiremen

Symbol	Parameter	-70		Unit
		Min	Max	
Tas	Address setup time	0		ns
t_{AW}	Address valid to end of write	70		ns
t_{CdZZ}	Chip deselect to ZZ# LOW	5		ns
t_{CW}	Chip enable to end of write	70		ns
t_{WC}	Write cycle time	70		ns
t_{WP}	Write pulse width	46		ns
t_{WR}	Write recovery time	0		ns
t_{ZZWE}	ZZ# LOW to WE# LOW	10	500	ns

- **Software Access Sequence**

The contents of the CR can be read or modified using a software access sequence. If the software access mechanism is used, CE2 can simply be tied to Vcc; the port line typically used for CE2 control purposes will no longer be required.

The CR is loaded using a four-step sequence consisting of two READ operations followed by two WRITE operations (see Figure 3). The READ sequence is virtually identical except that an asynchronous READ is performed during the fourth operation (see Figure 4).

The address used during all READ and WRITE operations is the highest address of the PSRAM device being accessed (3FFFFFh); the content of this address is not changed by using the software-access sequence.

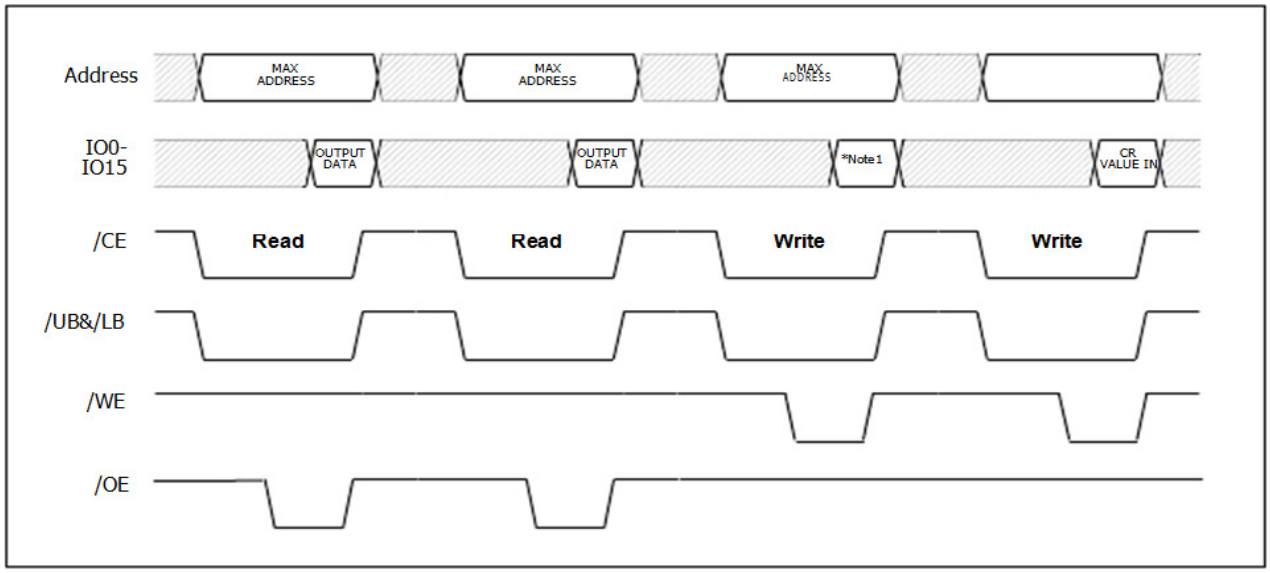
The data bus is used to transfer data into or out of bit [15:0] of the CR.

Writing to the CR using the software-access sequence modifies the function of the CE2. After the software sequence loads the CR, the level of the CE2 no longer enables PAR operation.

PAR operation is updated whenever the software-access sequence loads a new value into the CR. This CE2 functionality will remain active until the next time the device is powered up.

The operation of the CE2 is not affected if the software-access sequence is only used to read the contents of the CR. Use of the software-access sequence does not affect the performance of standard (CE2 controlled) CR loading.

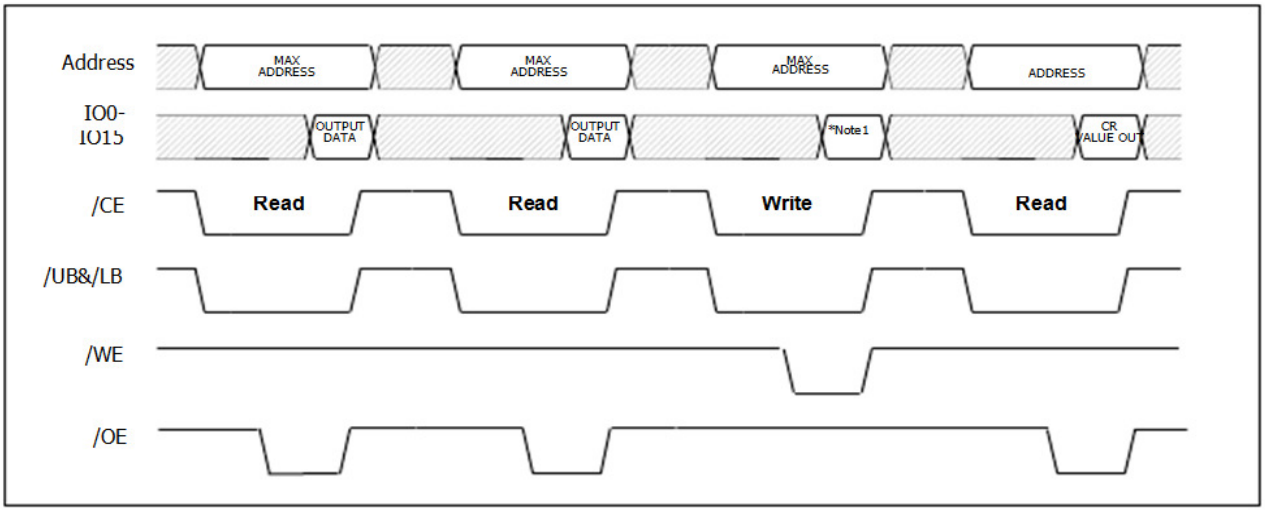
Figure 3 : Configuration Register Write



Notes :

1. CR : 0000h (CR [2:0] is 000; CR [4] is 0; CR [6:5] is 00 and CR [7] is 0)

Figure 4 : Configuration Register Read



Notes :

1. CR : 0000h (CR [2:0] is 000; CR [4] is 0; CR [6:5] is 00 and CR [7] is 0)

- **Partial-Array Refresh (PAR)**

The PAR bits restrict REFRESH operation to a portion of the total memory array. The refresh options are “full array (CR [2:0]=100)” and “ none of the array (CR [2:0]=000]).”

This feature enables the device to reduce standby current by refreshing only that part of the memory array that is absolutely necessary.

Read and WRITE operations are ignored during PAR operation.

The device only enters PAR mode if the sleep bit in the CR has been set HIGH (CR[4] = 1).

PAR can be initiated by taking the CE2 to the LOW voltage level for longer than 10us. Returning CE2 to HIGH will cause an exit from PAR, and the entire array will be immediately available for READ and WRITE operations.

- **Sleep Mode**

The sleep mode bit defines the low-power mode to be entered when CE2 is driven LOW. If CR [4] = 1, PAR operation is enabled. If CR [4] = 0, DPD operation is enabled.

DPD operation disables all refresh-related activity. When DPD is enabled, any stored data will become corrupted. When refresh activity has been re-enabled. The PSRAM device will require 150us to perform an initialization procedure before normal operation can resume.

- **Temperature Compensated Refresh (TCR)**

TCR register bits can be programmed using the CR [5:6] configuration registers and has four different temperature levels: +15℃, +45℃, +70℃, and +85℃. Default CR [5:6] value is 85℃.

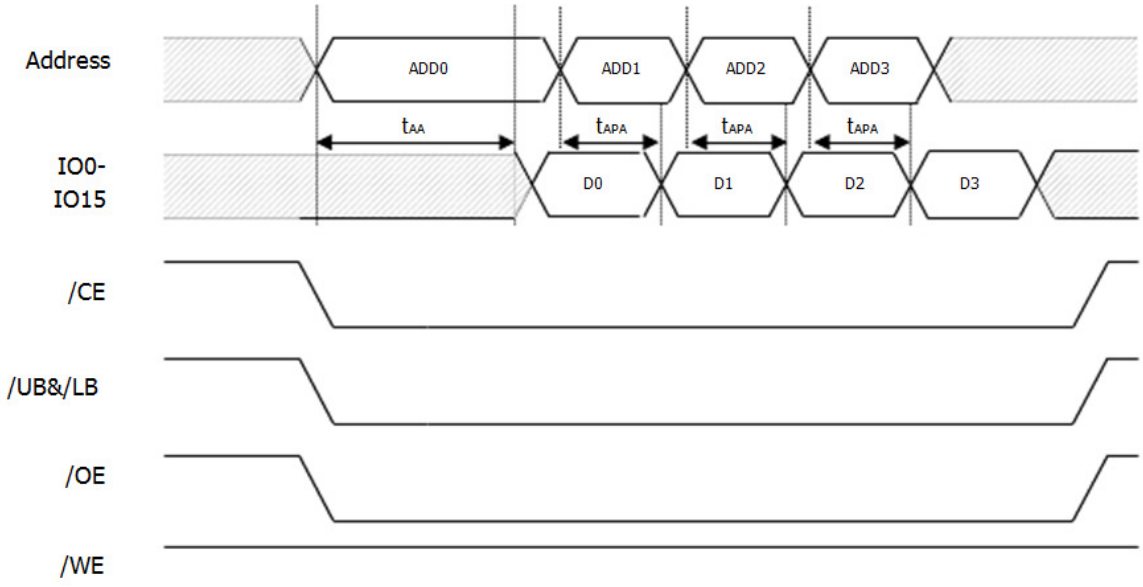
The temperature selected must be equal to or higher than the case temperature of the device. Setting a lower temperature level would cause data to be corrupted due to insufficient refresh rate.

- **Page Mode READ Operation**

Page mode is a performance-enhancing extension to the legacy asynchronous READ operation. In page-mode-capable products, an initial asynchronous read access is preformed, then adjacent addresses can be read quickly by simply changing the low-order address. Addresses A [3:0] are used to determine the members of the 16-address PSRAM page. Any change in addresses A [4] or higher will initiate a new tAA access time. Figure 5 shows the timing for a page mode access.

This mode takes advantage of the fact that adjacent addresses can be read faster than random addresses. WRITE operations do not include comparable page mode functionality. The /CE LOW time is limited by refresh considerations. /CE must not stay LOW longer than tCEM.

Figure 5. Page Mode READ Operation

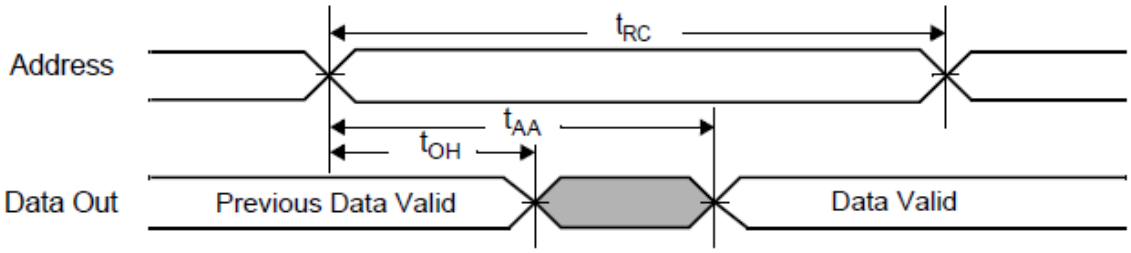


Read cycle

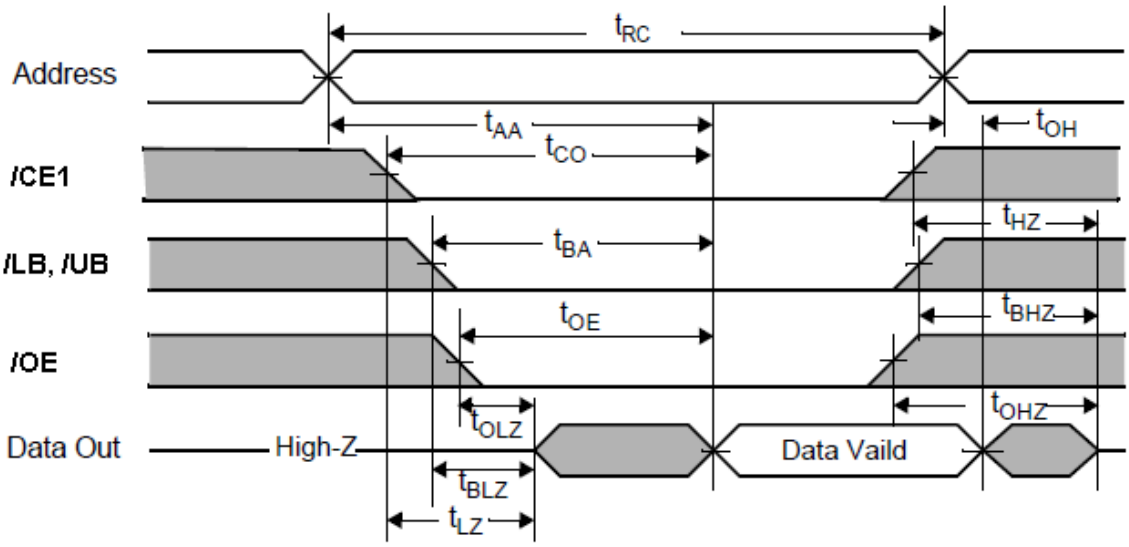
Parameter Name	Name	70		Unit
		Min	Max	
Read cycle time	t_{RC}	70	10,000	ns
Address access time	t_{AA}	-	70	ns
Maximum cycle time	t_{MRC}	-	10,000	
Page read cycle time	t_{PC}	25	-	ns
Page Address Access Time	t_{PAA}	-	25	ns
Chip enable access time (/CE1)	t_{CO}	-	70	ns
Output enable to output valid (/OE)	t_{OE}	-	25	ns
Byte enable access time	t_{BA}	-	70	ns
Output hold from address change	t_{OH}	5	-	ns
Chip enable to output in low Z (/CE1)	t_{LZ}	10	-	ns
Output enable to output in low Z (/OE)	t_{OLZ}	3	-	ns
Byte enable to output in low Z	t_{BLZ}	10	-	ns
Chip disable to output in High Z (/CE1)	t_{HZ}	-	20	ns
Output disable to output in High Z (/OE)	t_{OHZ}	-	20	ns
Byte disable to output in High Z	t_{BHZ}	-	20	ns
Maximum CE# pulse width[1]	t_{CEM}			

1. Page mode enable only

READ CYCLE (1) (Address controlled, /CE1=/OE=VIL, CE2=/WE=VIH, /UB or/and /LB=VIL)



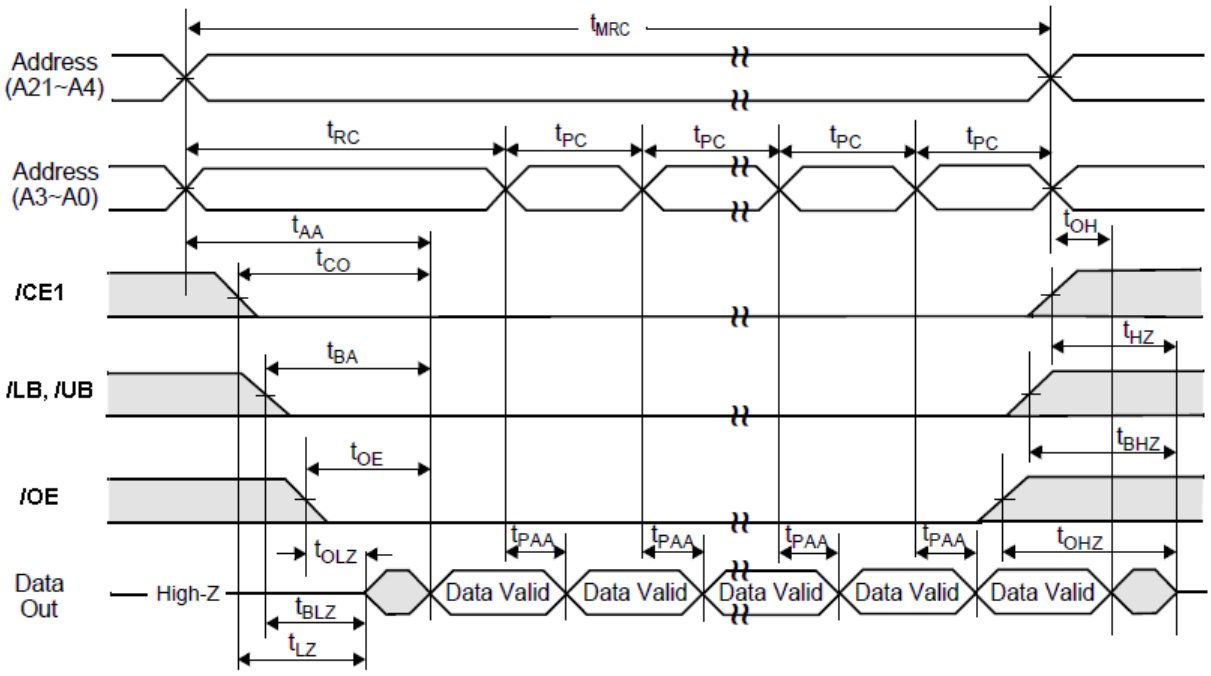
READ CYCLE (2) (CE2=/WE=VIH)



NOTES (READ CYCLE)

1. tHZ , tBHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. Do not Access device with cycle timing shorter than tRC for continuous periods > 10us.

PAGE READ CYCLE (2) (CE2=/WE=VIH, 16 Words access)



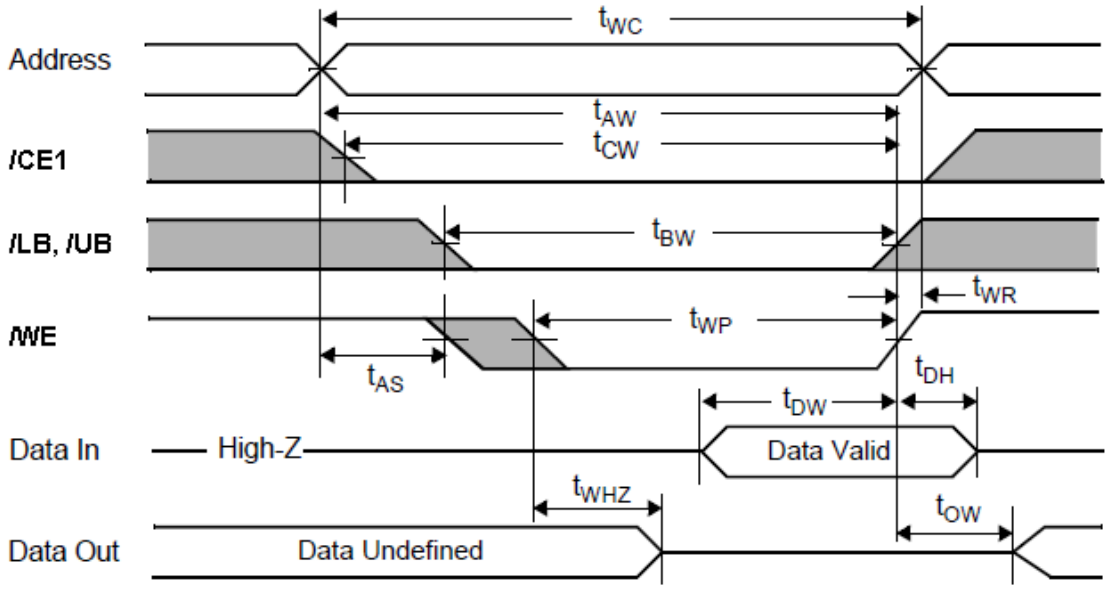
NOTES (READ CYCLE)

1. tHZ , tBHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. Do not Access device with cycle timing shorter than tRC for continuous periods > 10us.

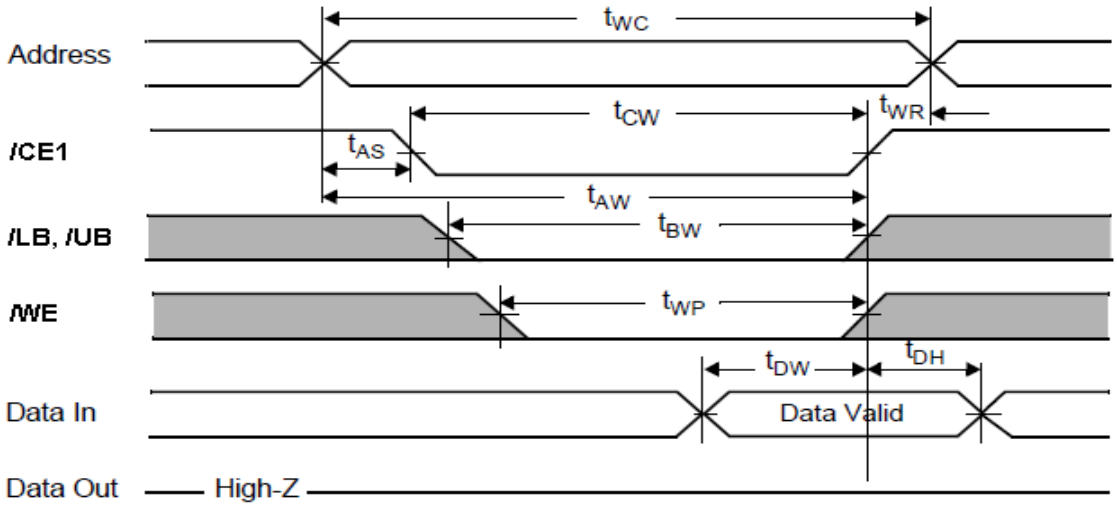
Write Cycle

Parameter Name	Name	70		Unit
		Min	Max	
Write cycle time	t_{WC}	70	10,000	ns
Byte enable to end of write	t_{BW}	70	-	ns
Address valid to end of write	t_{AW}	70	-	ns
Chip select to end of write	t_{CW}	70	-	ns
Data set up time	t_{DW}	23	-	ns
Data hold time	t_{DH}	0	-	ns
Write pulse width	t_{WP}	50	-	ns
Address set up time	t_{AS}	0	-	ns
Write recovery time(/WE)	t_{WR}	0	-	ns
/WE high to output low Z	t_{OW}	5	-	ns
Write to output high Z	t_{WHZ}	0	20	ns

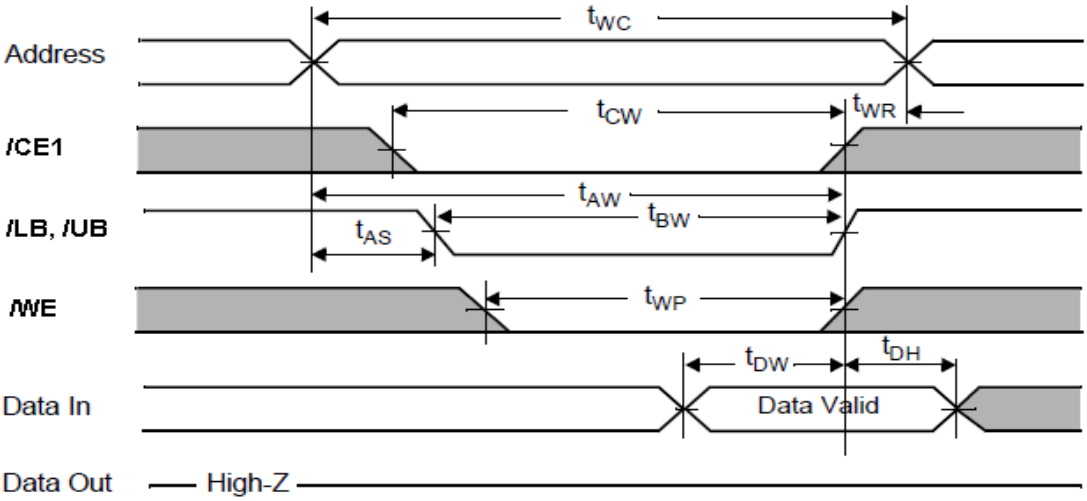
WRITE CYCLE (1) (/WE controlled, CE2=VIH)



WRITE CYCLE (2) (/CE1 controlled, CE2=VIH)



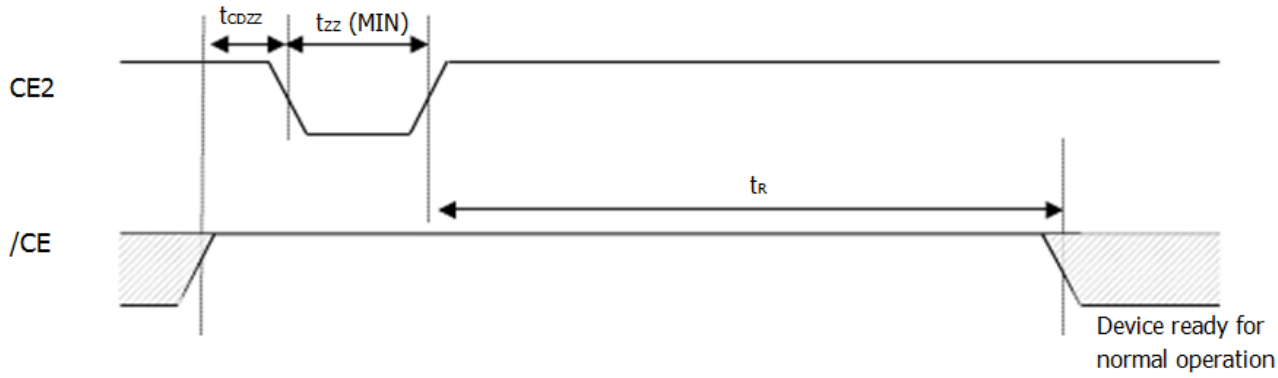
WRITE CYCLE (3) (/LB, /UB controlled, CE2=VIH)



NOTES (WRITE CYCLE)

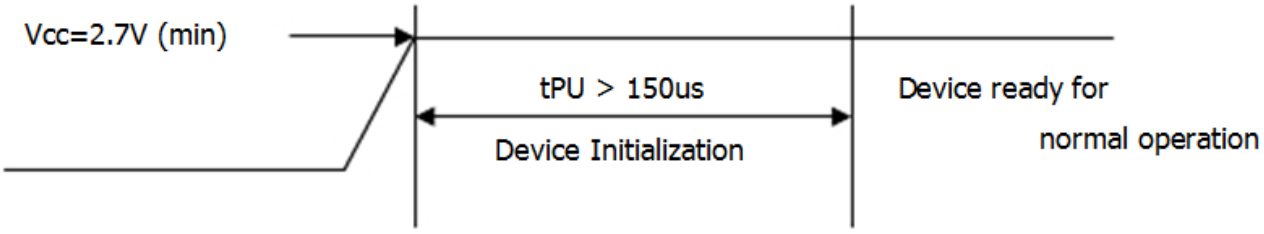
1. A write occurs during the overlap(tWP) of low /CE1, low /WE and low /UB or /LB. A write begins at the last transition among low /CE1 and low /WE with asserting /UB or /LB low for single byte operation or simultaneously asserting /UB and /LB low for word operation. A write ends at the earliest transition among high /CE1 and high /WE. The tWP is measured from the beginning of write to the end of write.
2. tCW is measured from /CE1 going low to end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR applied in case a write ends as /CE1 or /WE going high.
5. Do not access device with cycle timing shorter than tWC for continuous periods > 10us.

Deep Power-Down Mode Entry / Exit



Symbol	Parameter Name	-70		Unit
		Min	Max	
t_{CDZZ}	Chip deselect to CE2 LOW	5		ns
t_R	Deep Power-down recovery	150		us
t_{ZZ} (Min)	Minimum CE2 pulse width	10		us

■ TIMING WAVEFORM OF POWER UP



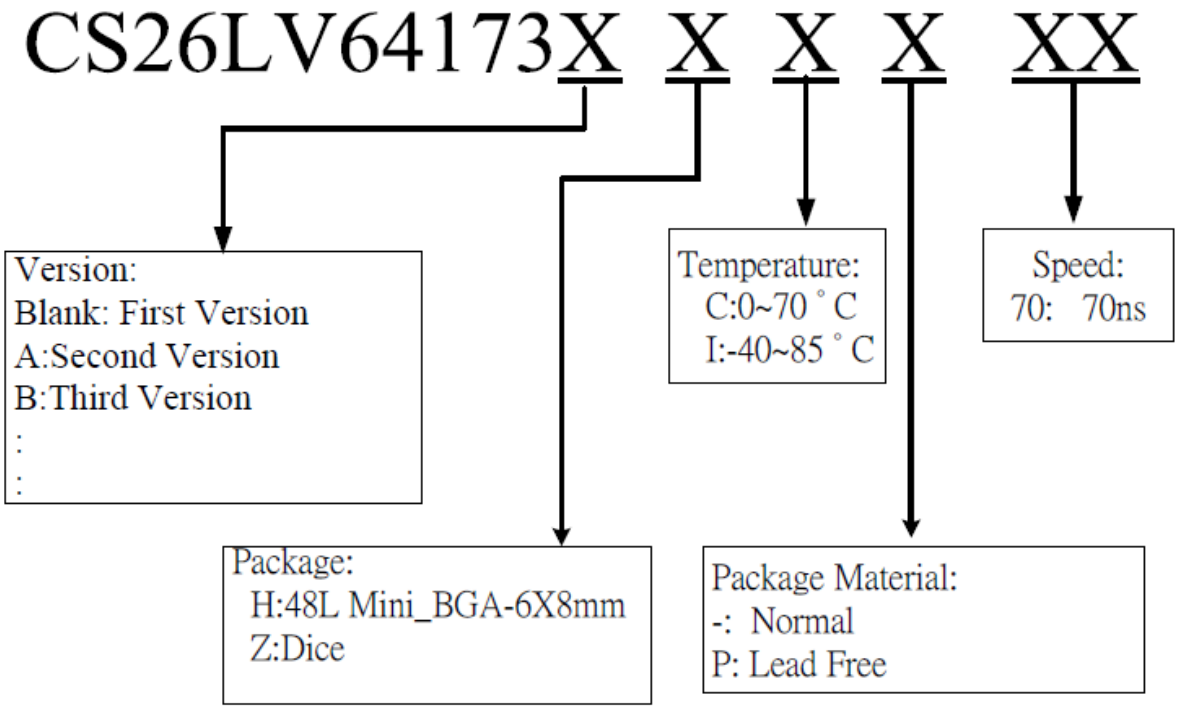
Symbol	Parameter	-70		Unit
		Min	Max	
t_{PU}	Initialization Period (required before normal operations)		150	us

PSRAM products include an on-chip voltage sensor that is used to launch the power-up initialization process. Initialization will load the CR with its default settings (see Table 1).

Vcc must be applied simultaneously. When they reach a stable level above 2.7V, the device will require 150μs to complete its self-initialization process (see above picture).

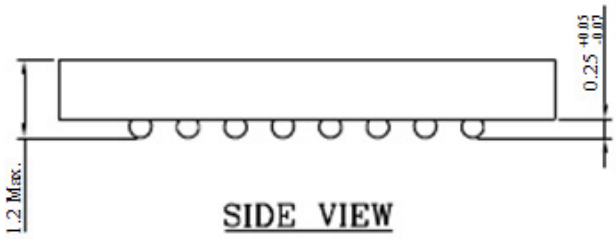
During the initialization period, /CE should remain HIGH. When initialization is complete, the device is ready for normal operation.

■ Order Information

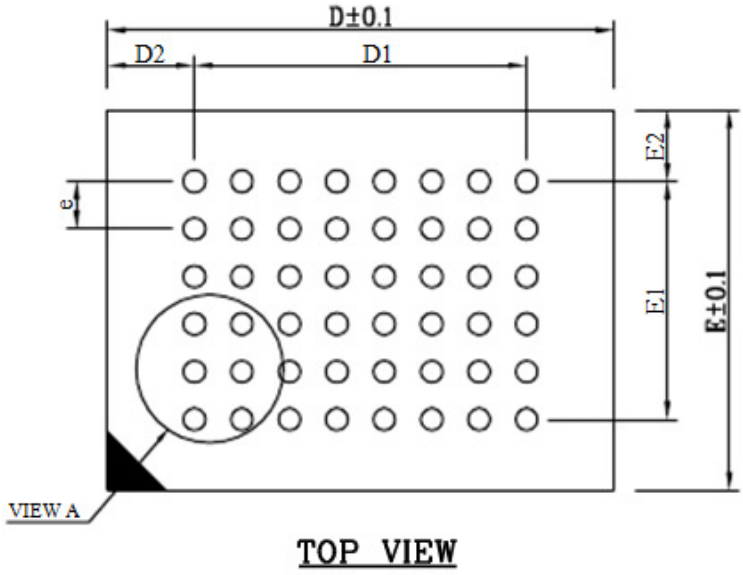


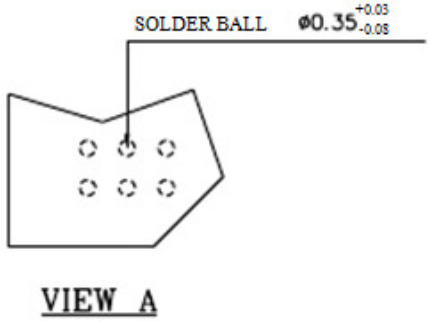
Note: Package material code “P” meets ROHS

PACKAGE DIMENSIONS: 48 ball Mini_BGA-6x8mm



BALL PITCH e = 0.75						
D	E	N	D1	E1	D2	E2
8.0	6.0	48	5.25	3.75	1.375	1.125





NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
2. PIN#1 DOT MARKING BY LASER OR PAD PRINT.
3. SYMBOL "N" IS THE NUMBER OF SOLDER BALLS.
4. TOLERANCES:

   LINEAR : X.X = ±0.1

   X.XX = ± 0.05

   X.XXX = ± 0.025